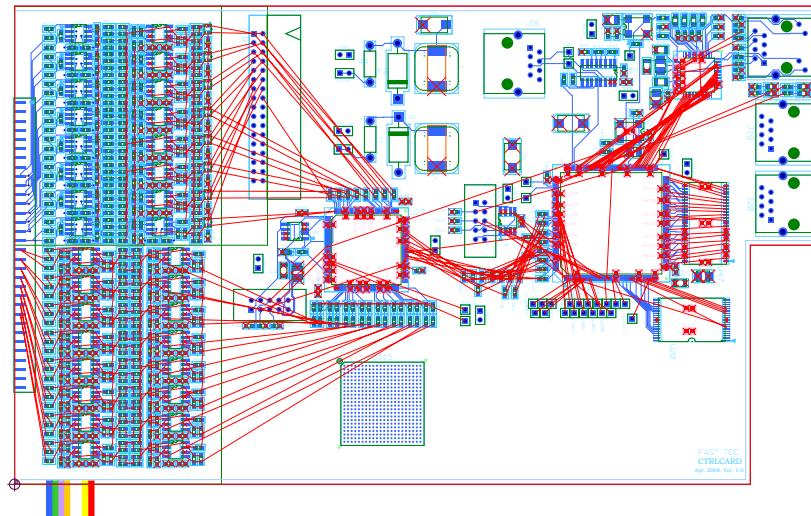


Digitizationat Feed Through (1): Printed Circuit Design



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In This Talk...

- Review the Digitization Process,
- Compare the new and old designs for the pulse shaper portion of the fast TDC control card,
- Discuss the changes made to the pulse shaper,
- Review the implementation options for comparator/TDC,
- Preview the layout changes made to the fast TDC control card,
- Show the new design for the Ethernet control.

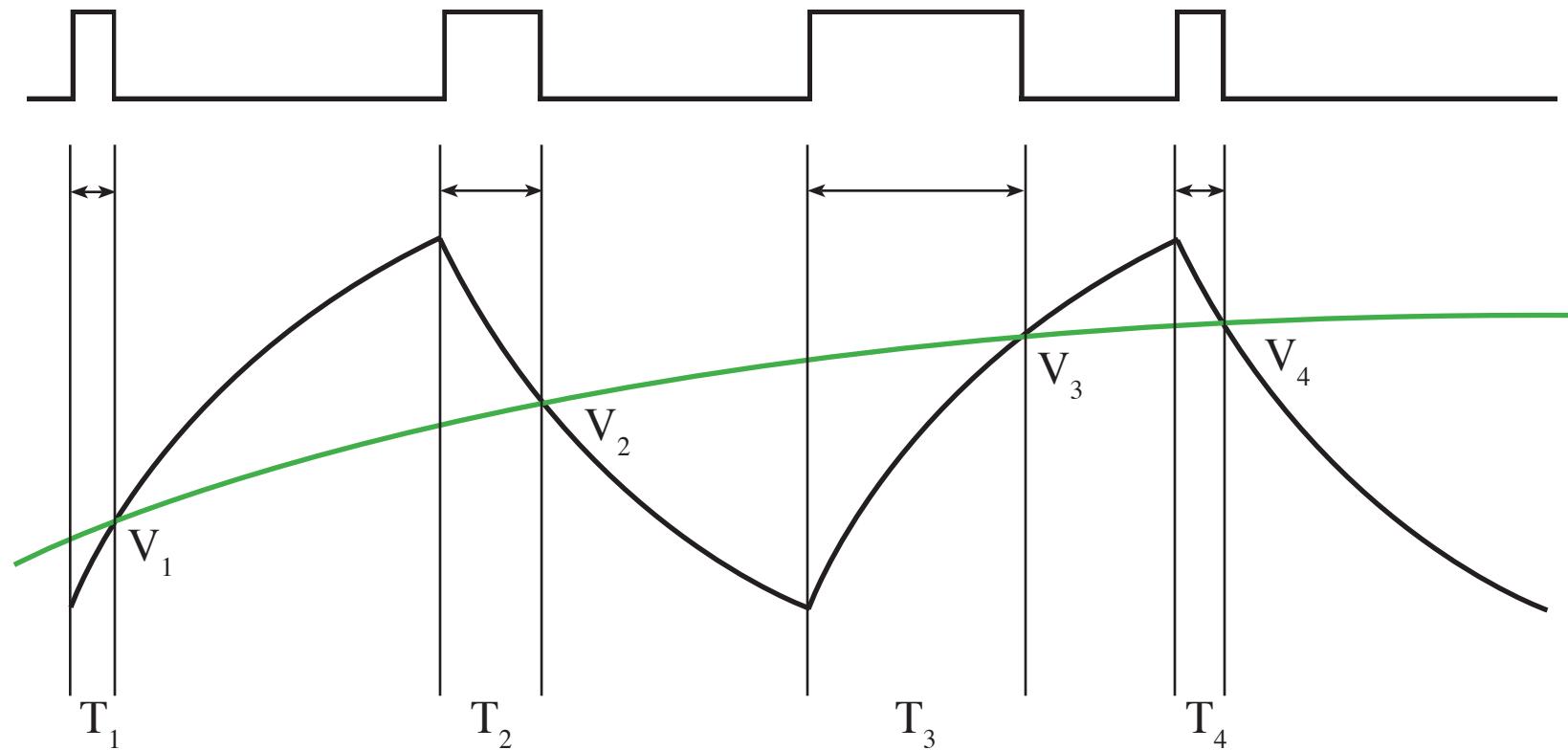
Digitization

Our main motivating factor for the Fast TDC control card is to reduce noise.

- The digitization will occur immediately after the feed through,
- Differential circuits will be used to minimize noise from the digitization process,
- Early digitization will allow for a longer cable run.

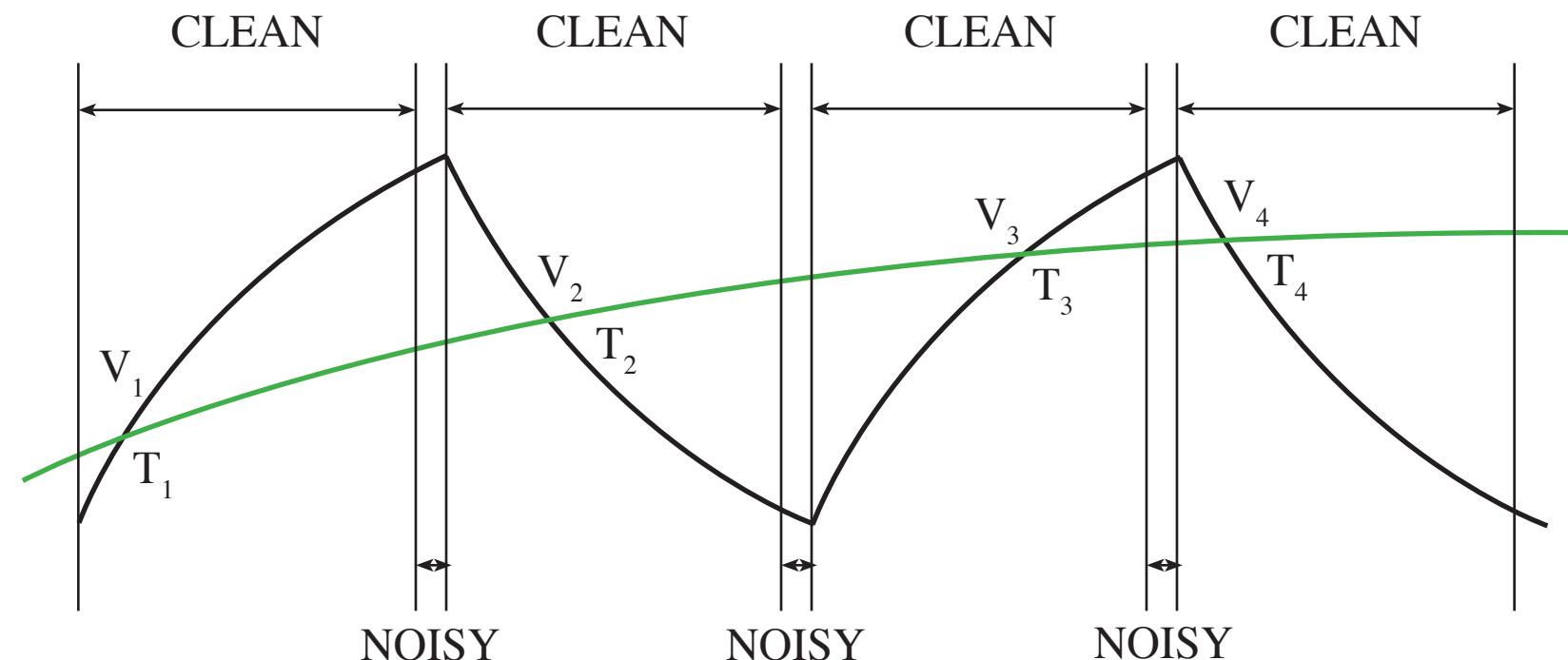
Digitization

- The analog signal is fed into a comparator and compared with a common reference voltage,
- Pulses rather than analog signals are transmitted on the cable.

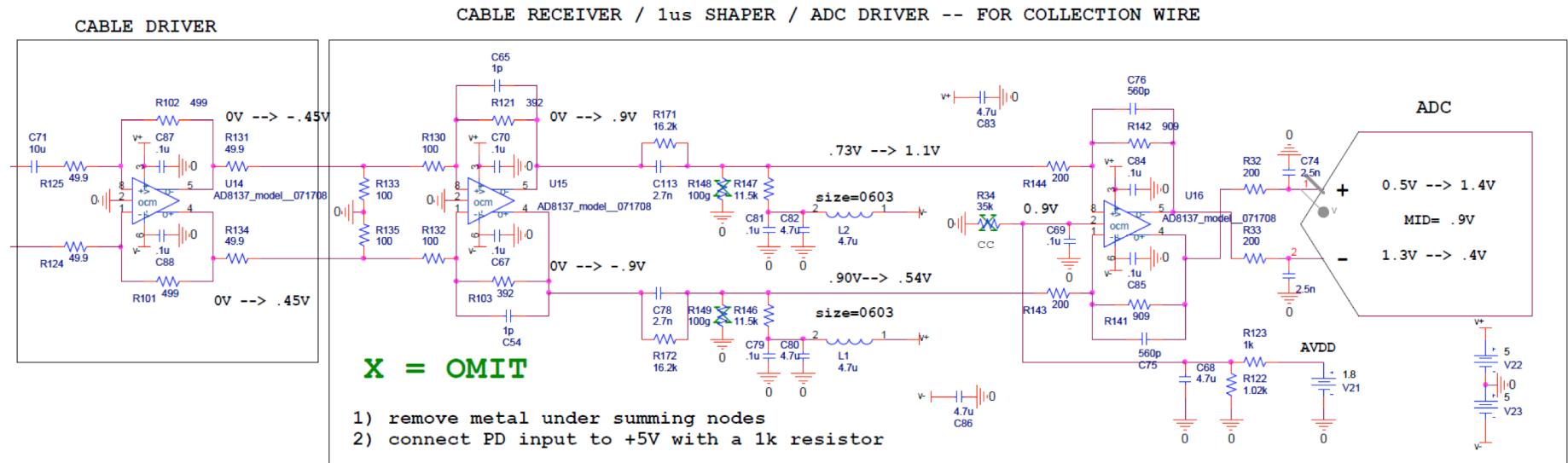


Digitization

- The analog signal can be reconstructed using the known reference voltage and the time samples,
- The time interval while the reference voltage changes from ramping up to ramping down may be noisy but the analog signal is not sampled during it.



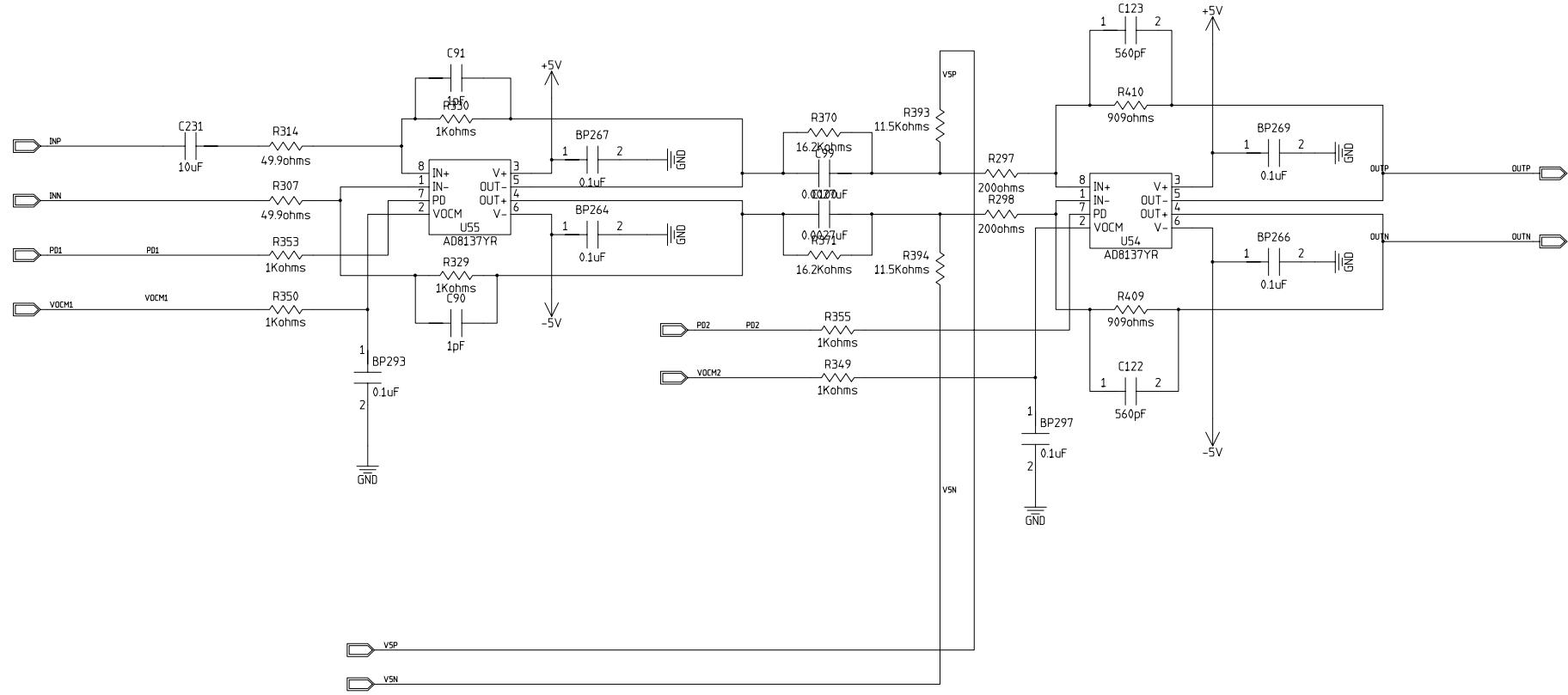
Pulse Shaper



Old design was a three stage amplifier:

- Its function is to prepare the analog signal before feeding it into the ADC,
 - This design was too large to fit onto the current board size,
 - I wanted to reduce space needed for the pulse shaper without compromising its function.

Pulse Shaper



New design is a two stage amplifier:

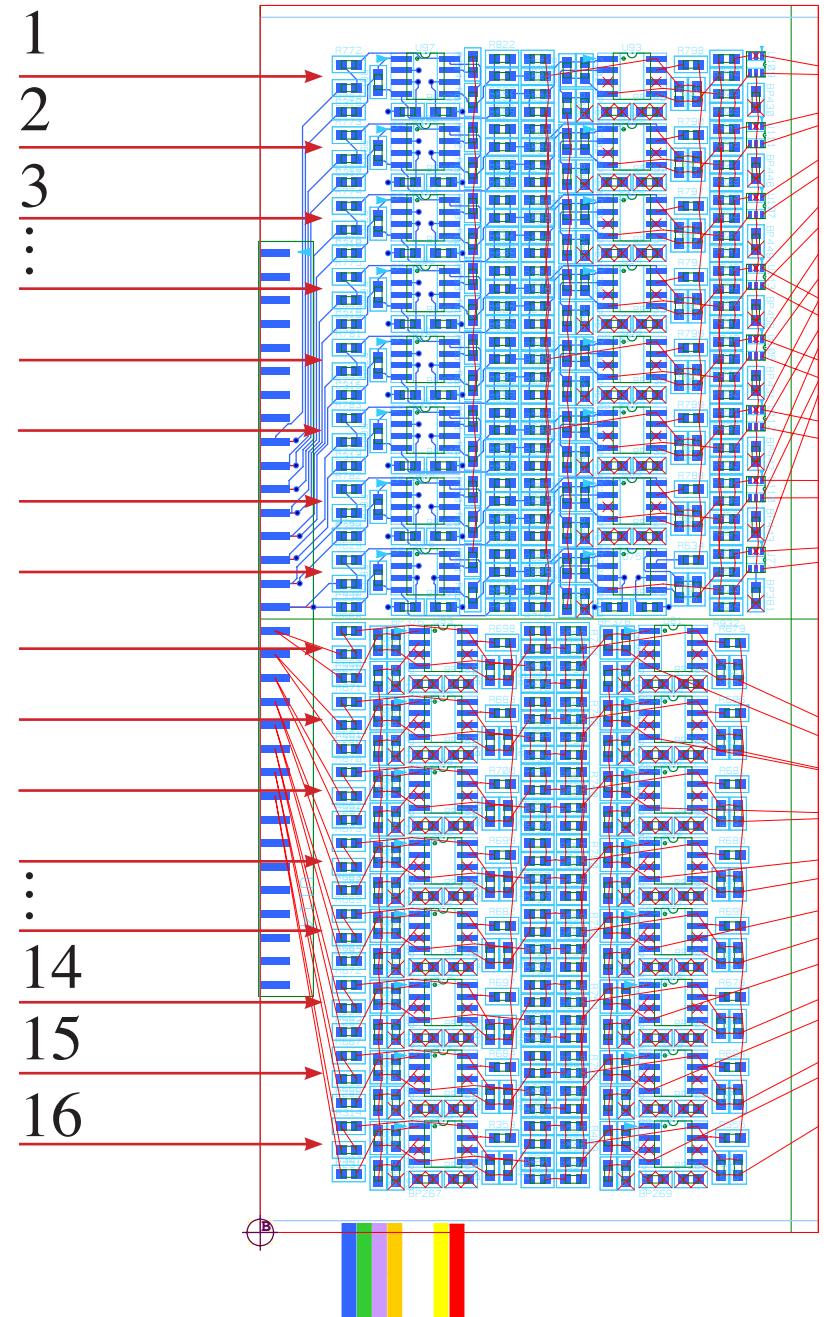
- Combined the first two opamps while preserving gain,
- Now feeds directly into a comparator,

Pulse Shaper

We eliminated enough components on the design to fit 16 pulse shapers on each side of the Fast TDC control card.

There are now enough pulse shapers for all the channels of input signal that the board will handle.

The next step on the control card is the comparator and TDC.

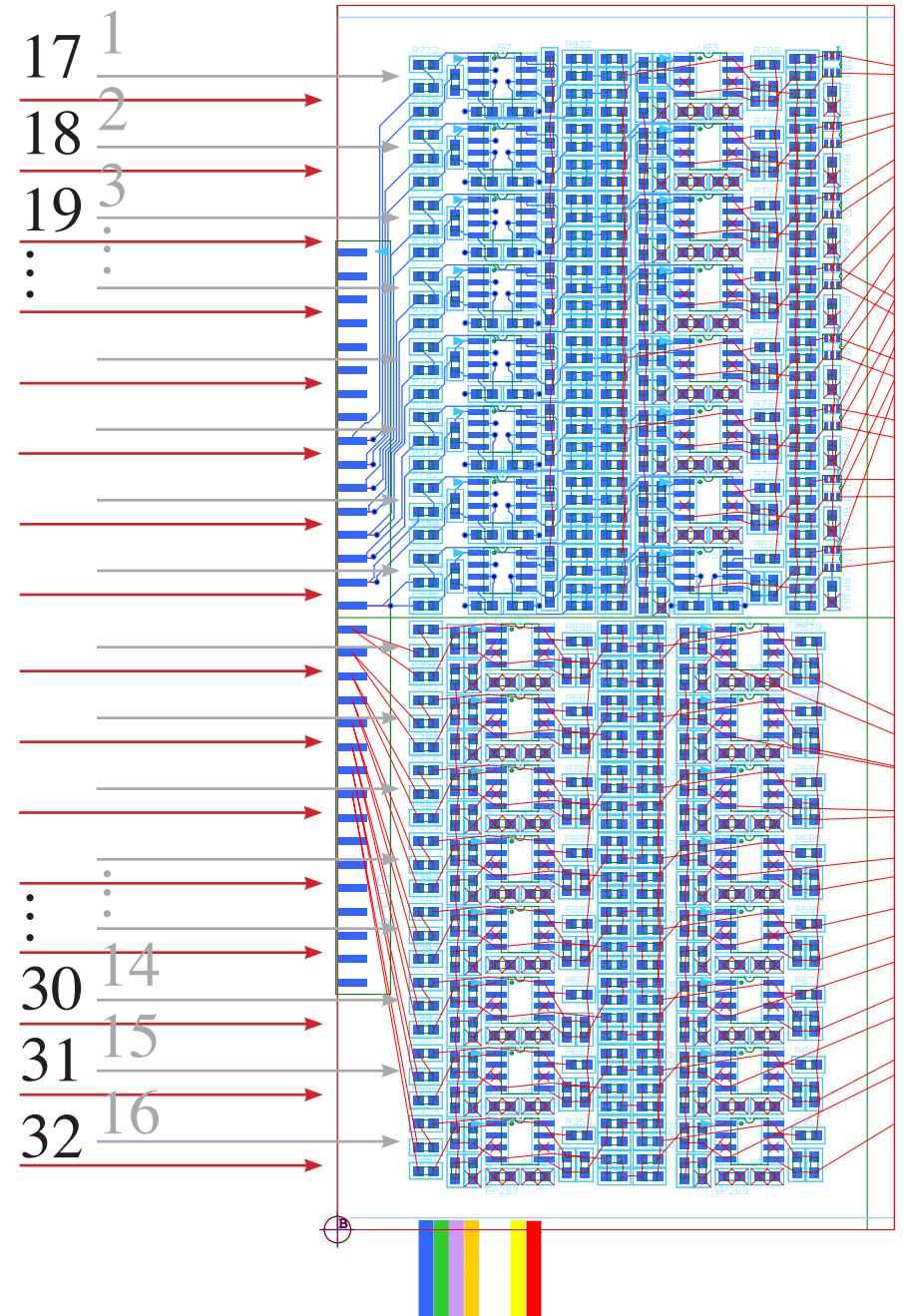


Pulse Shaper

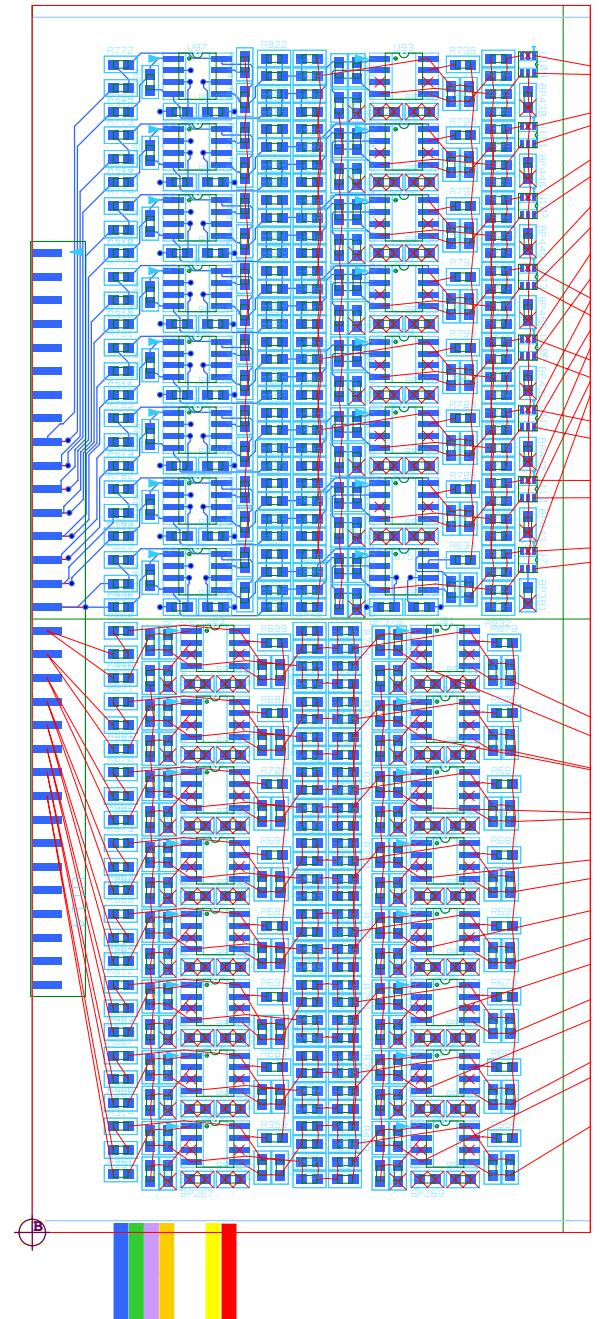
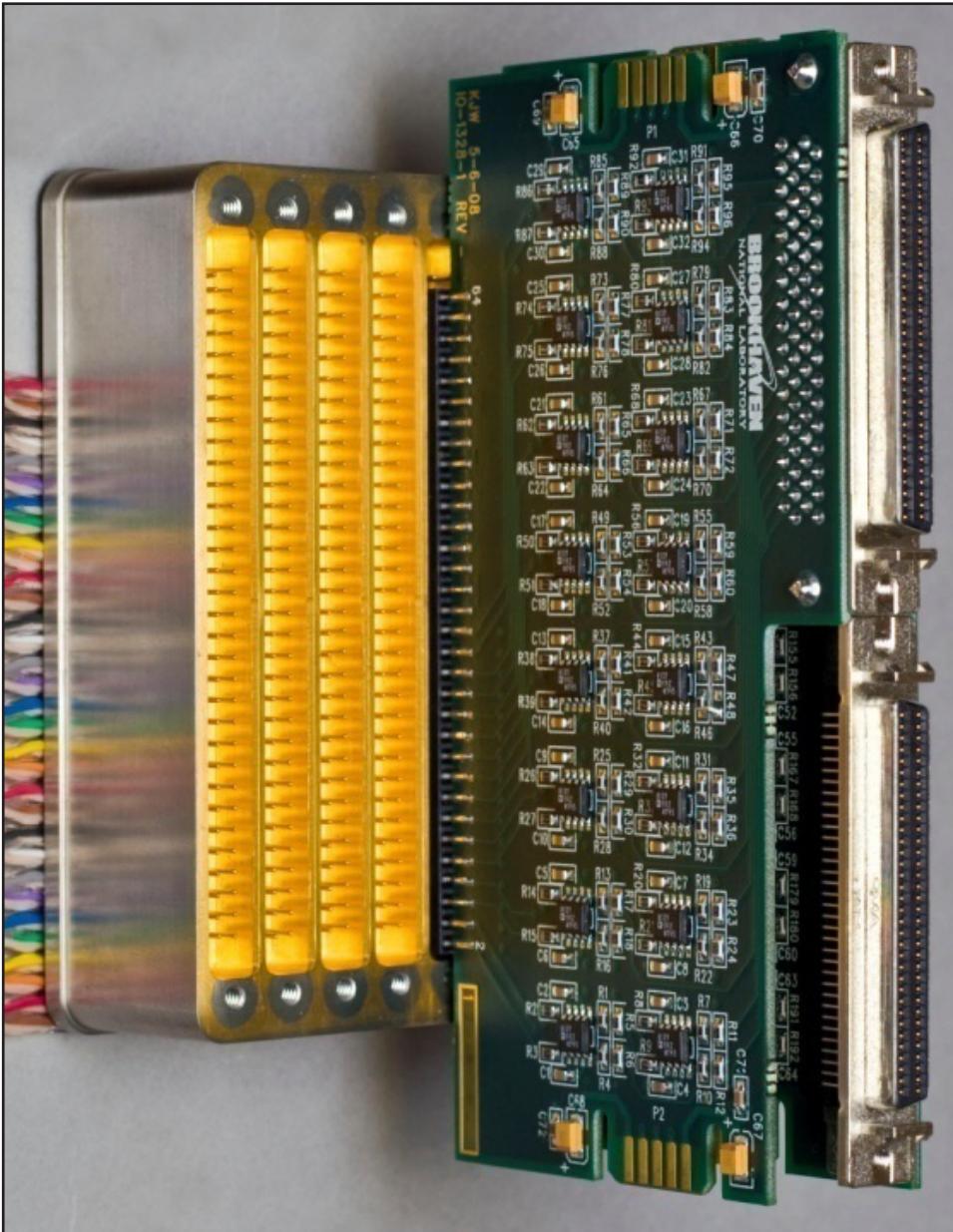
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Pulse Shaper



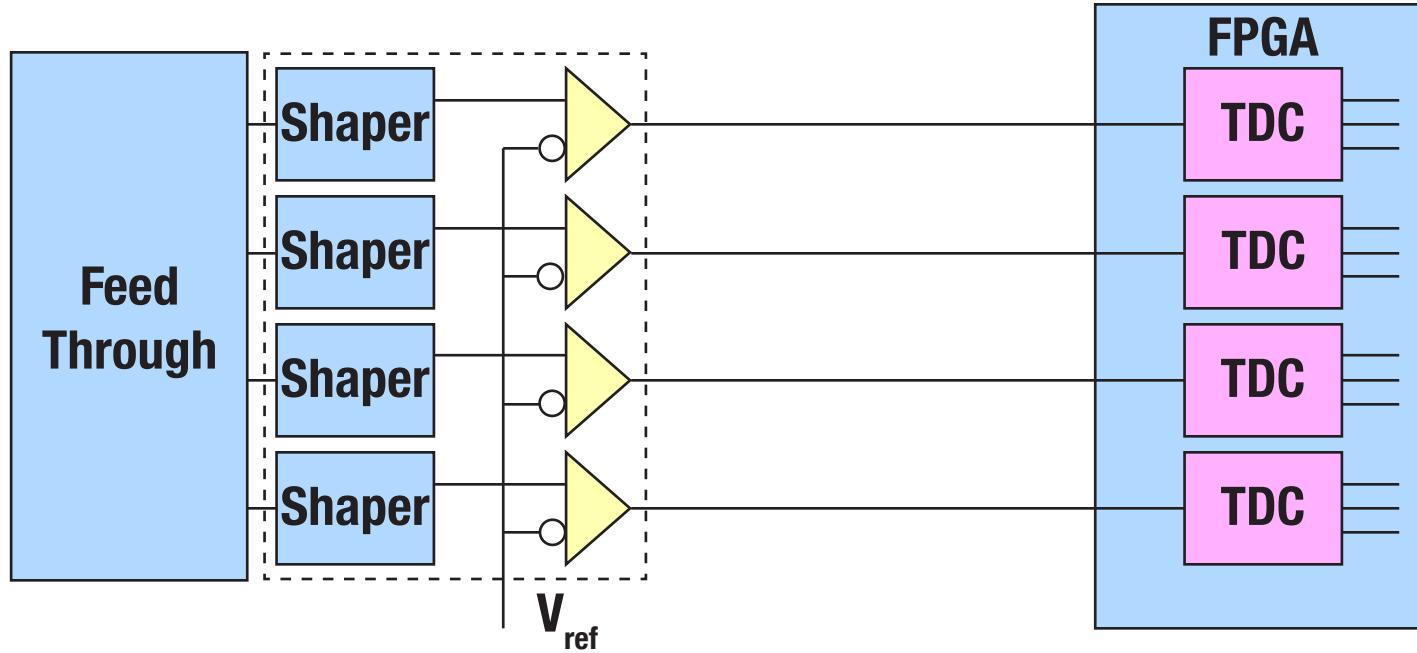
Comparator/TDC Options

There are three comparator implementation options that we plan on including on this board for testing:

Each option uses the FPGAs in different manners and includes the comparator at different points in the design.

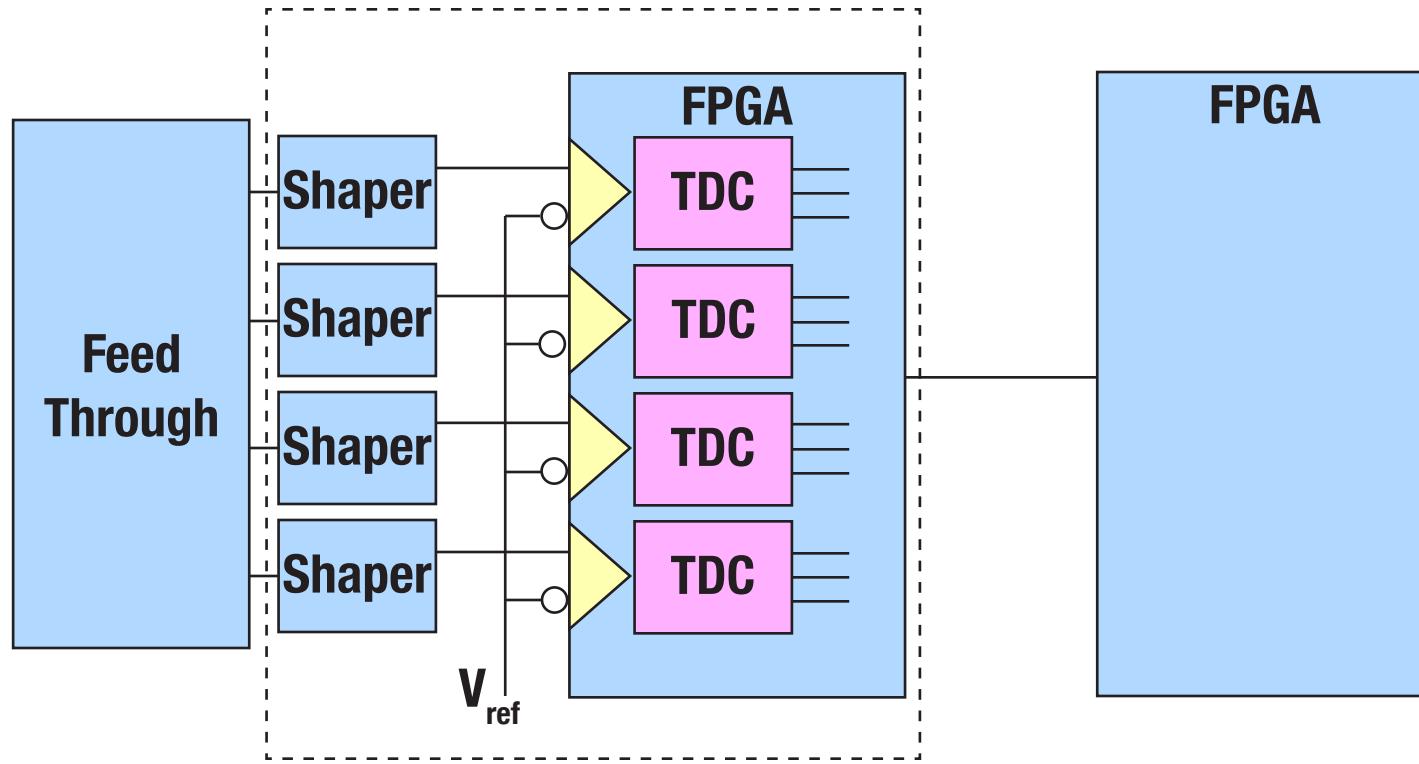
The current plan is to include all three of these options on this control card so that they can be tested and a final decision can be made on which one will be used.

Option I



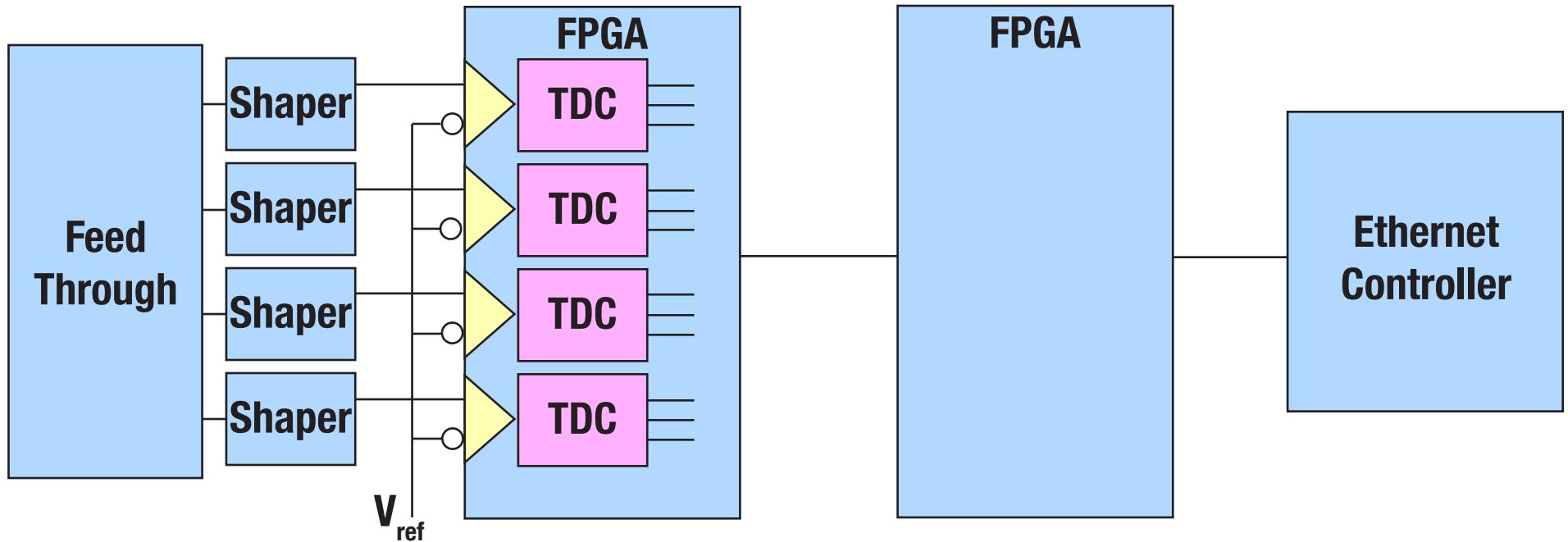
- The pulse shaper and reference voltage feeds directly into separate comparators that precedes the FPGA ,
- The TDC is programmed onto the FPGA that follows the comparators.

Option II

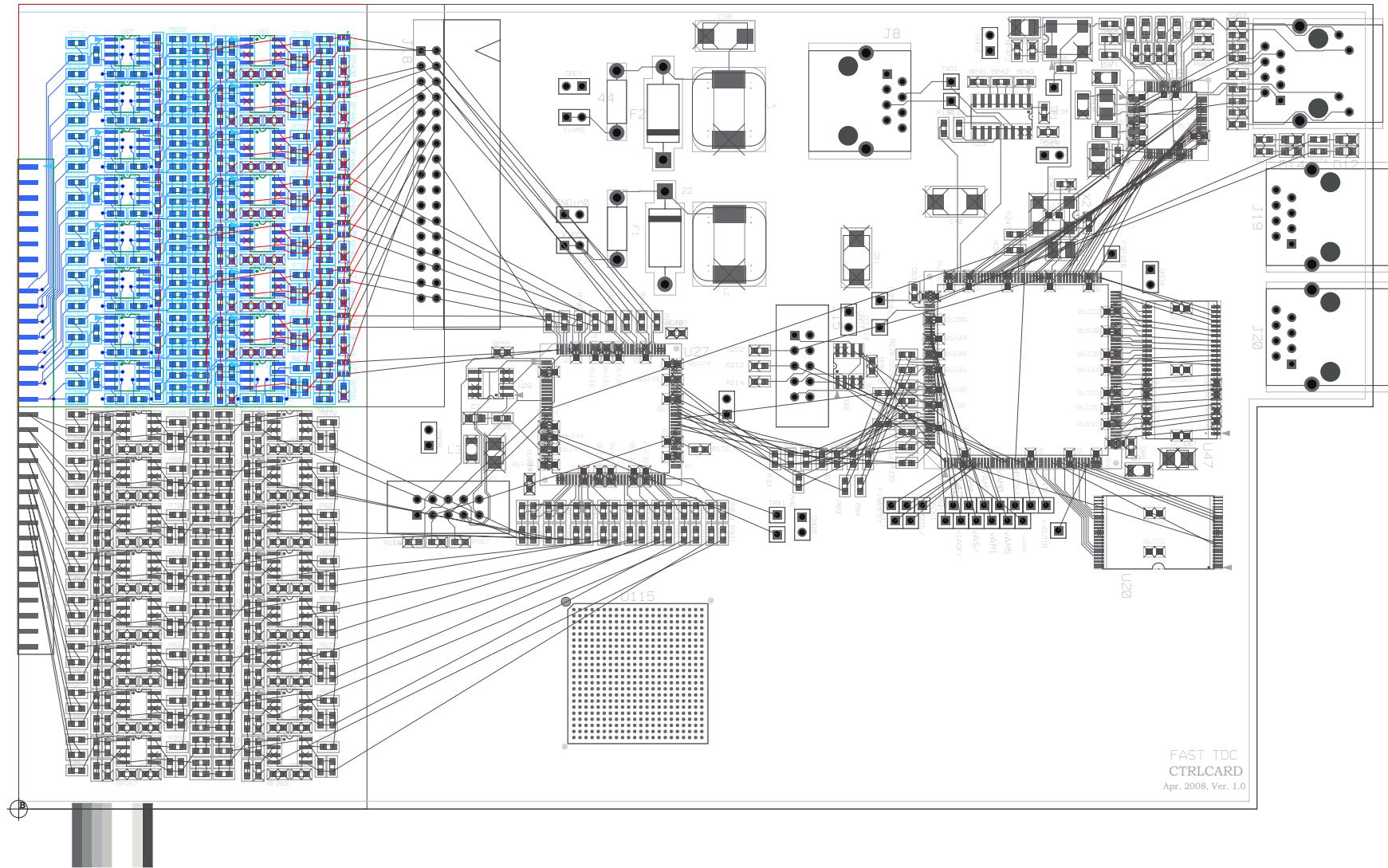


- The comparator is no longer a separate component from the first FPGA,
- The comparator and the TDC will be programmed onto the same FPGA where the analog signal and reference voltage will be sent after leaving the pulse shaper.

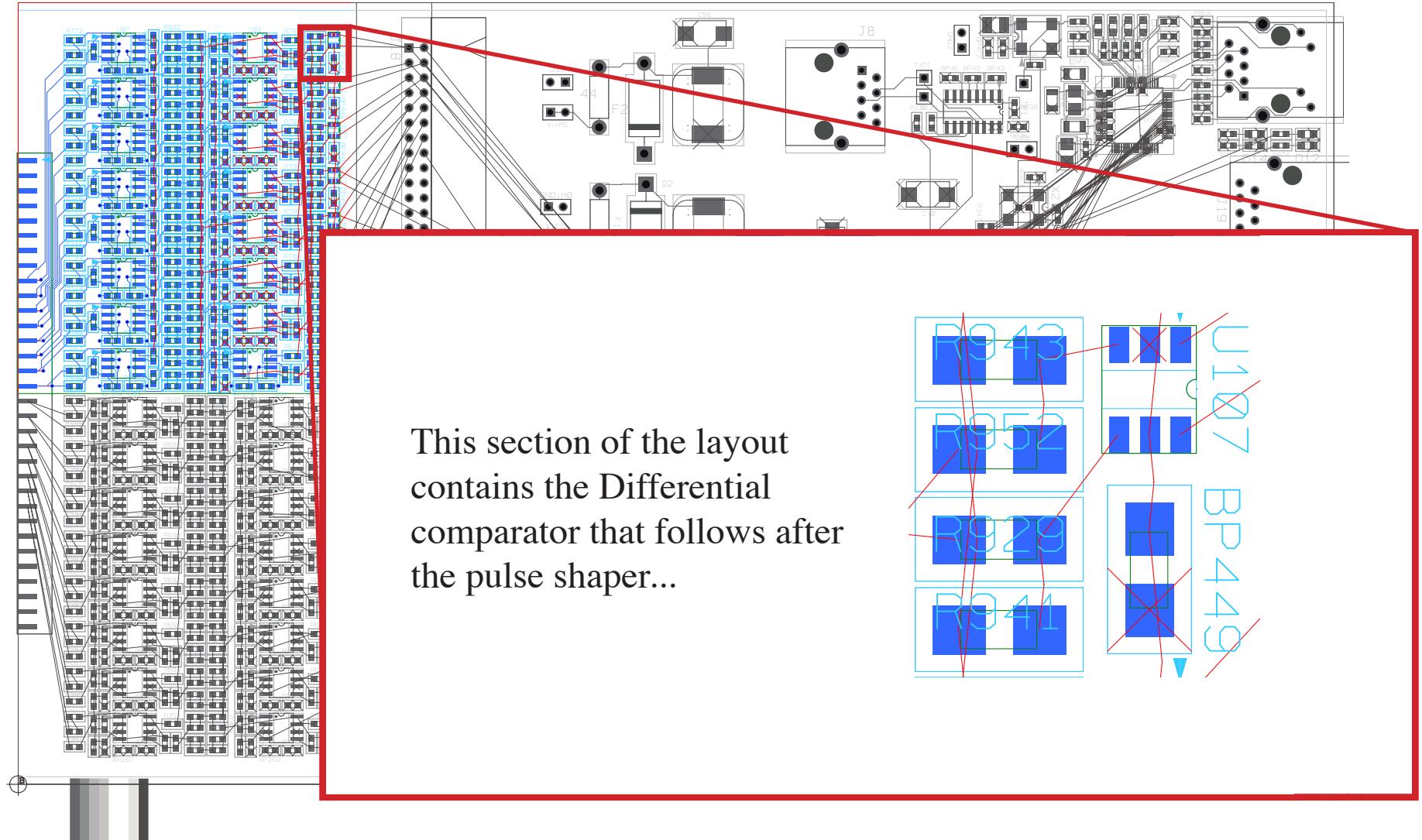
Option III



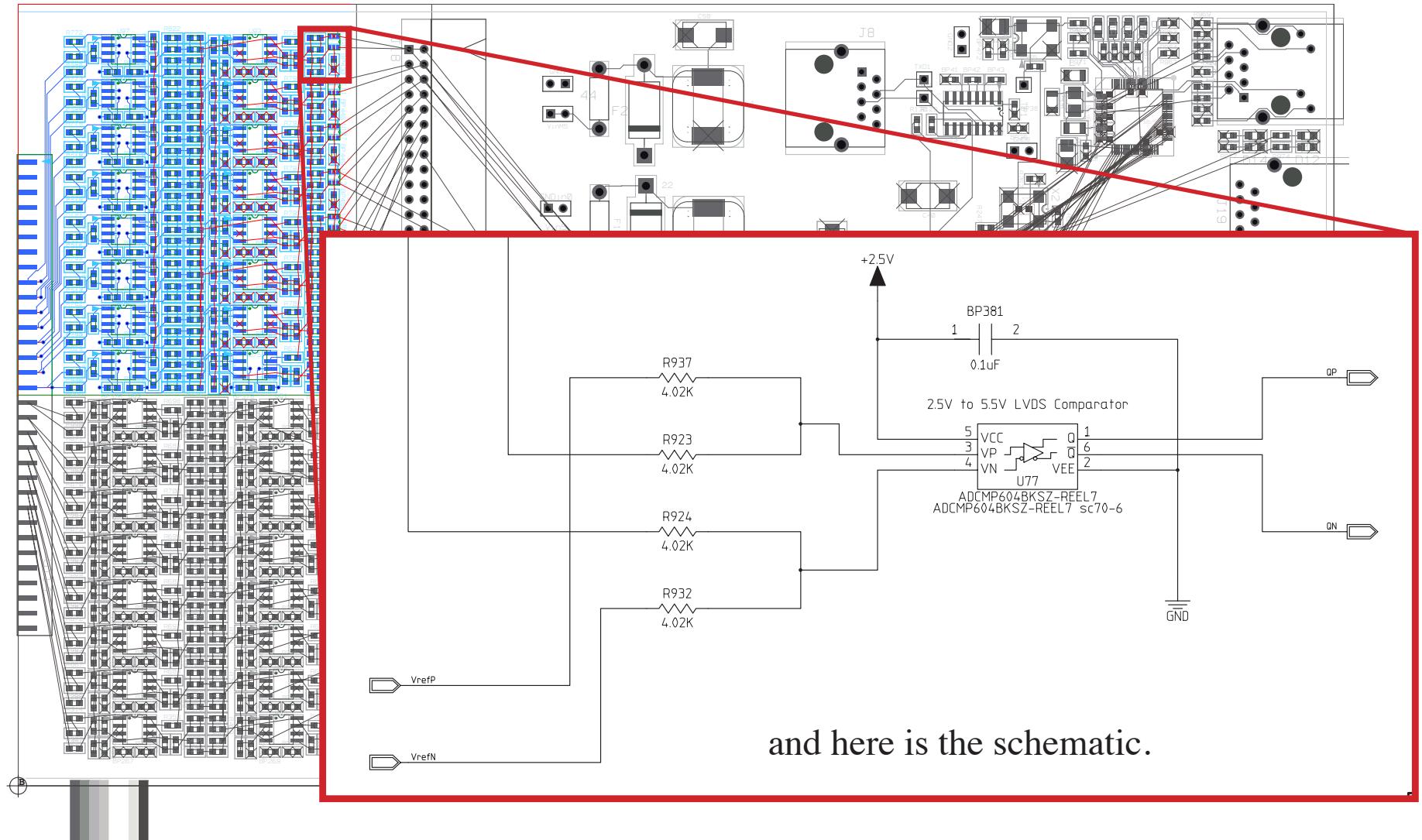
- Sends the digitized signal via Ethernet instead of serial port,
- Can use either of the previous comparator options.



Option I on the new layout

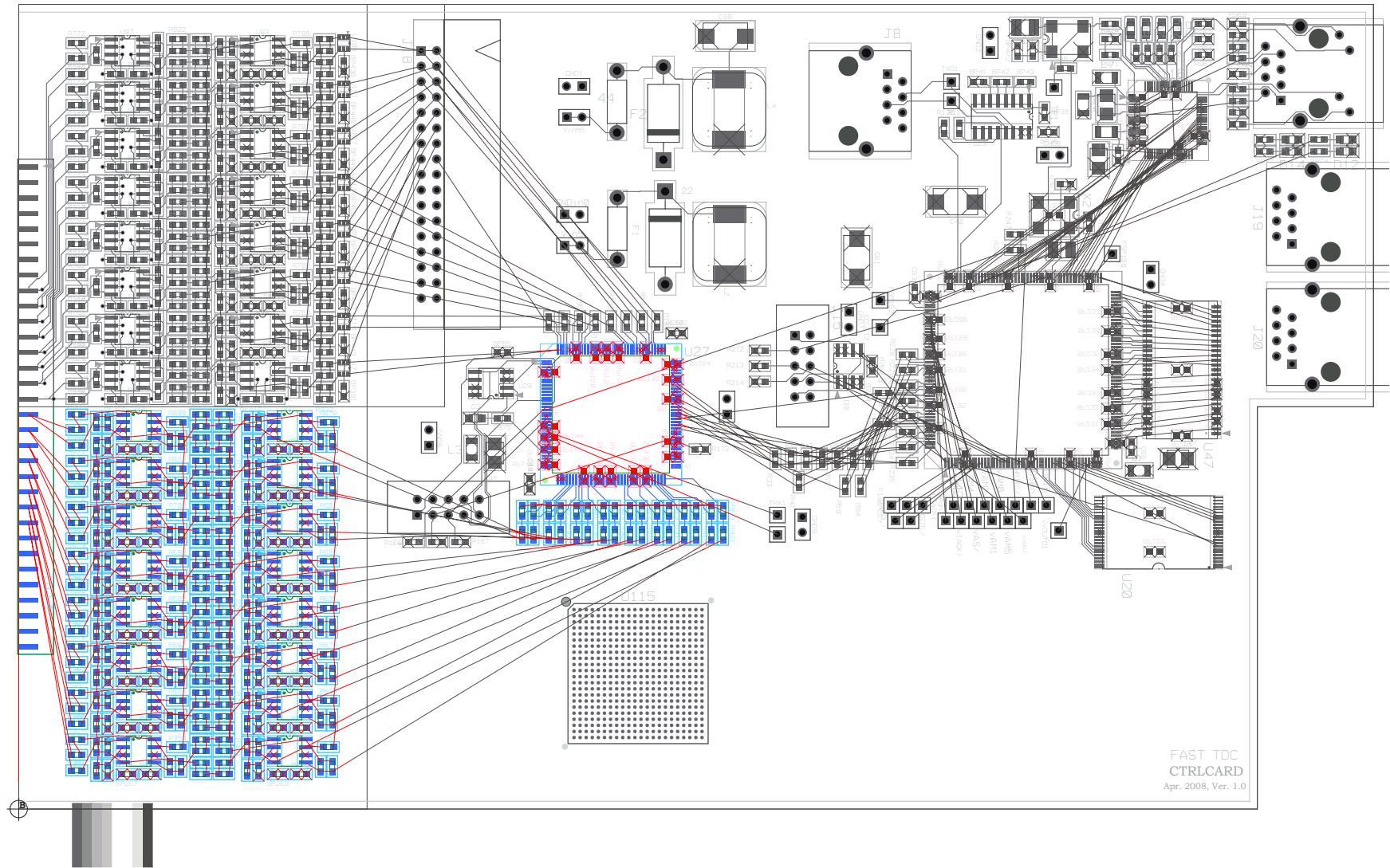


Option I on the new layout

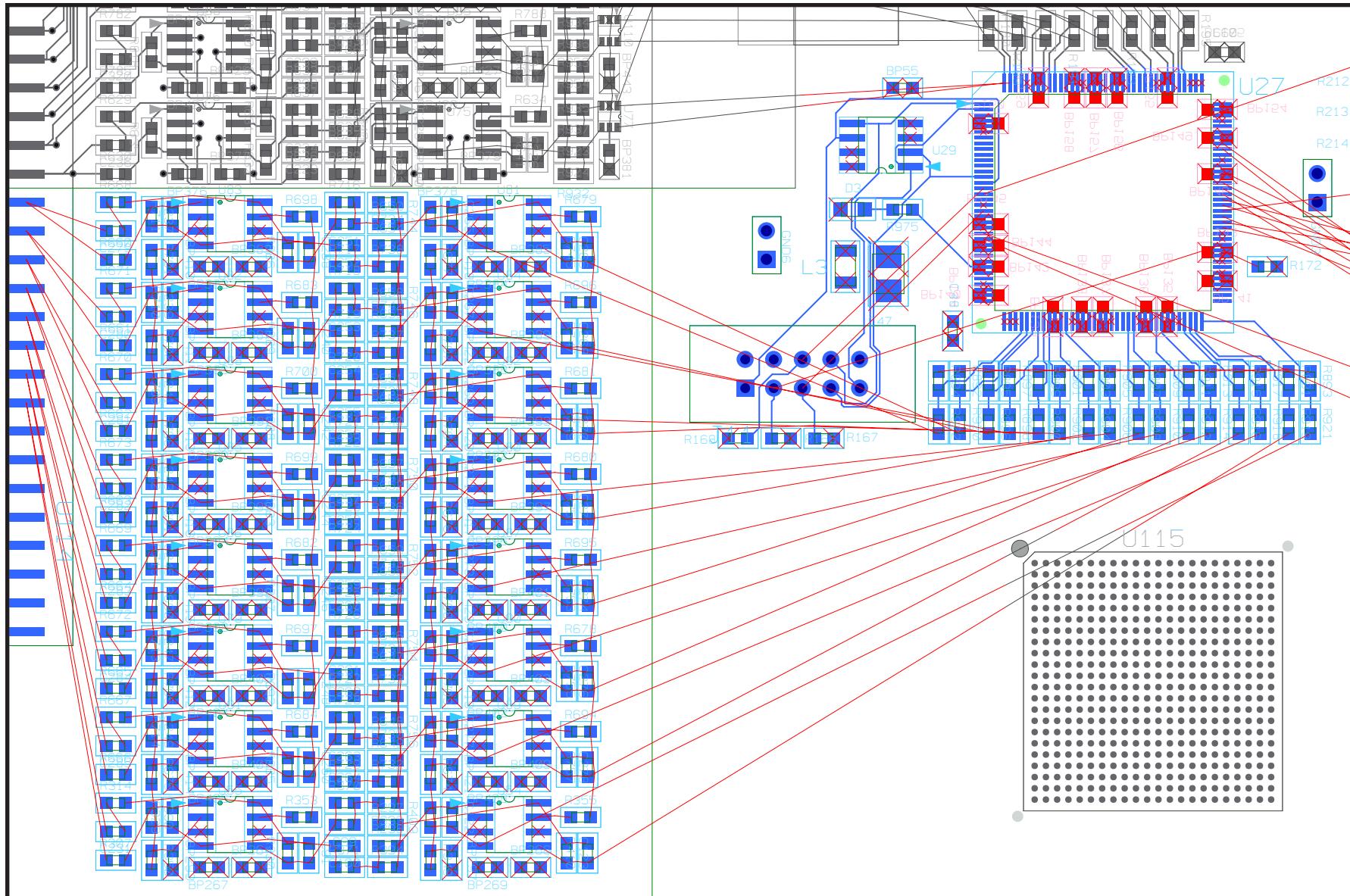


and here is the schematic.

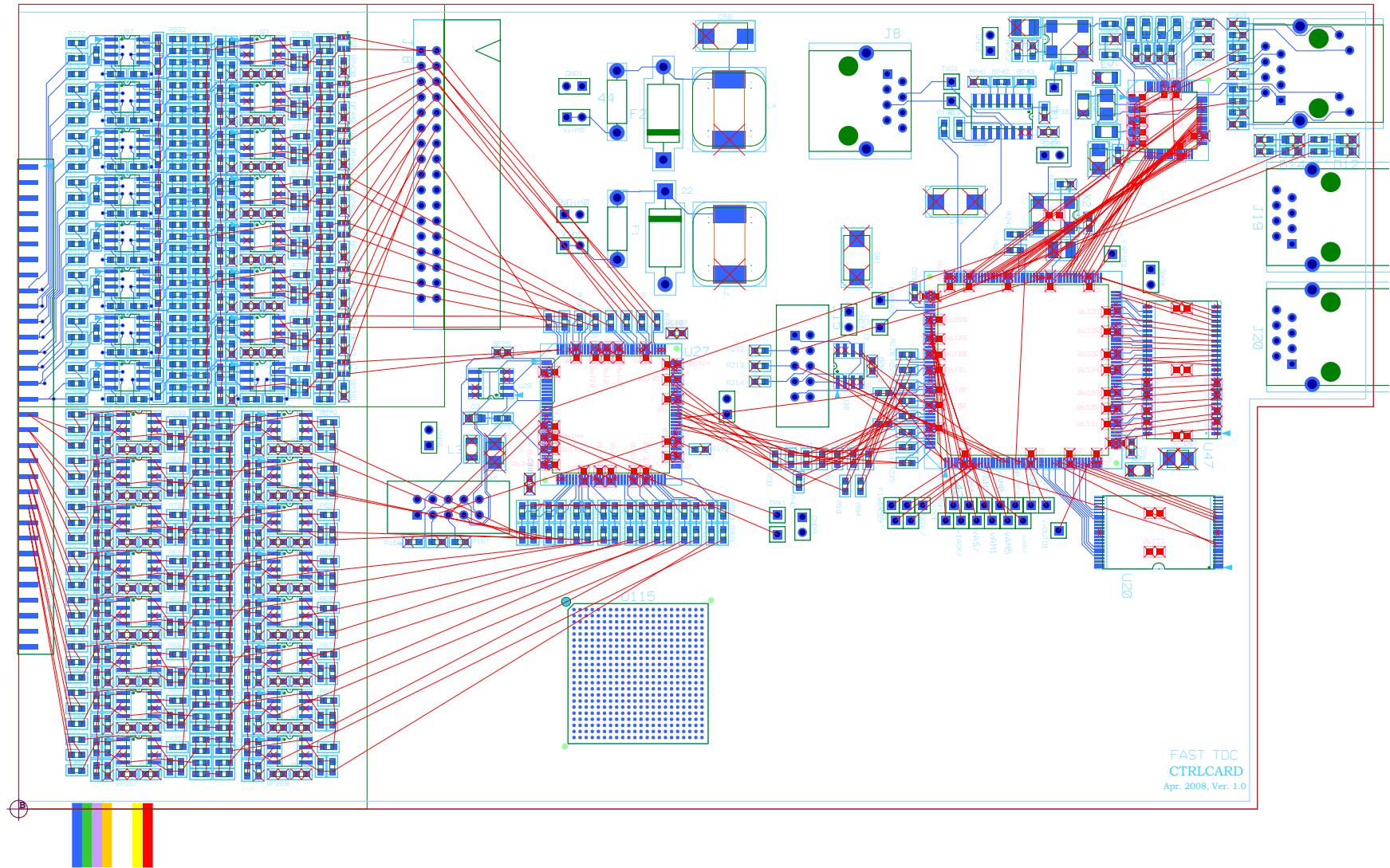
Option I on the new layout



Option II on the new layout

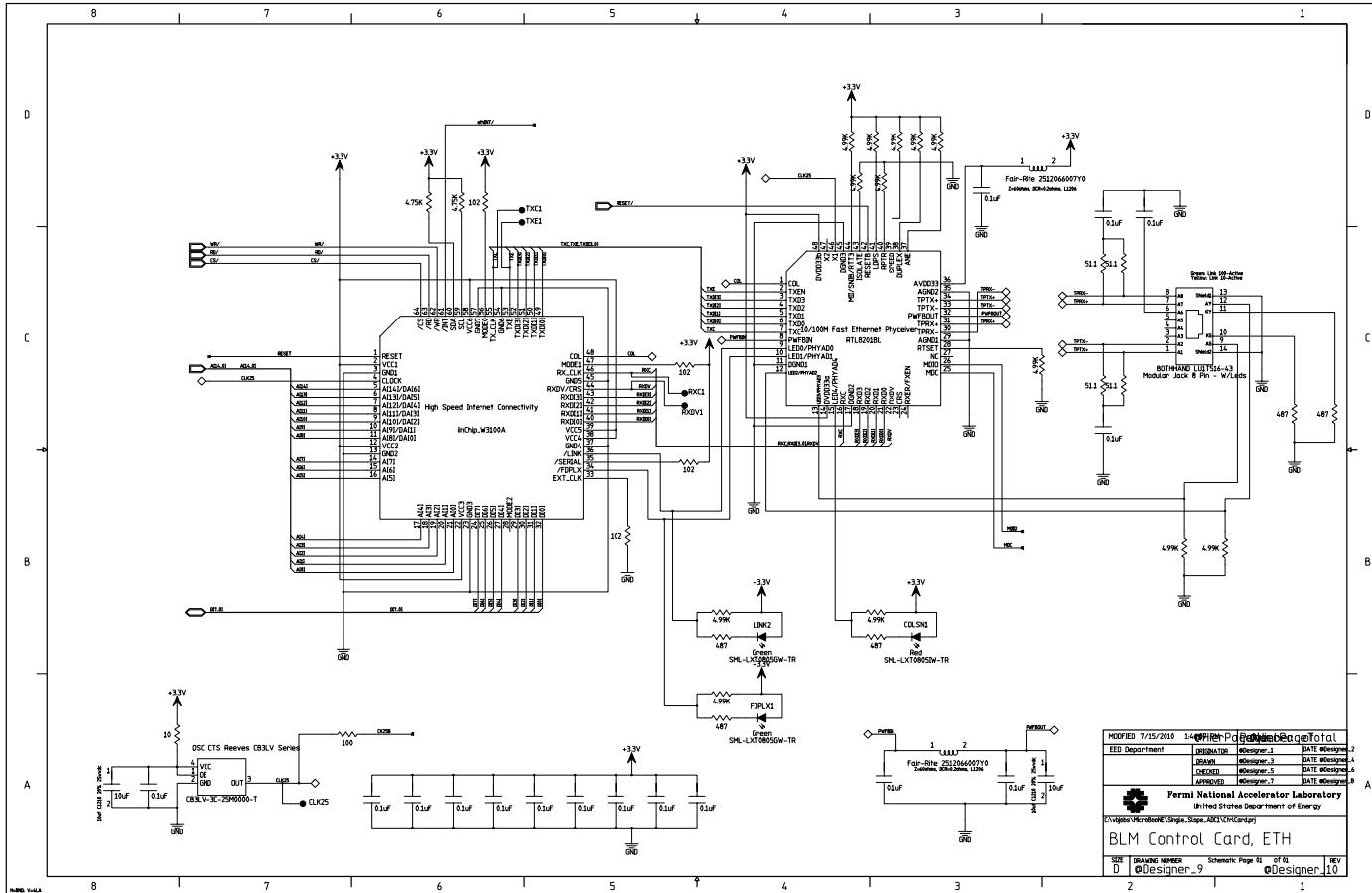


Option II on the new layout



Option III on the new layout

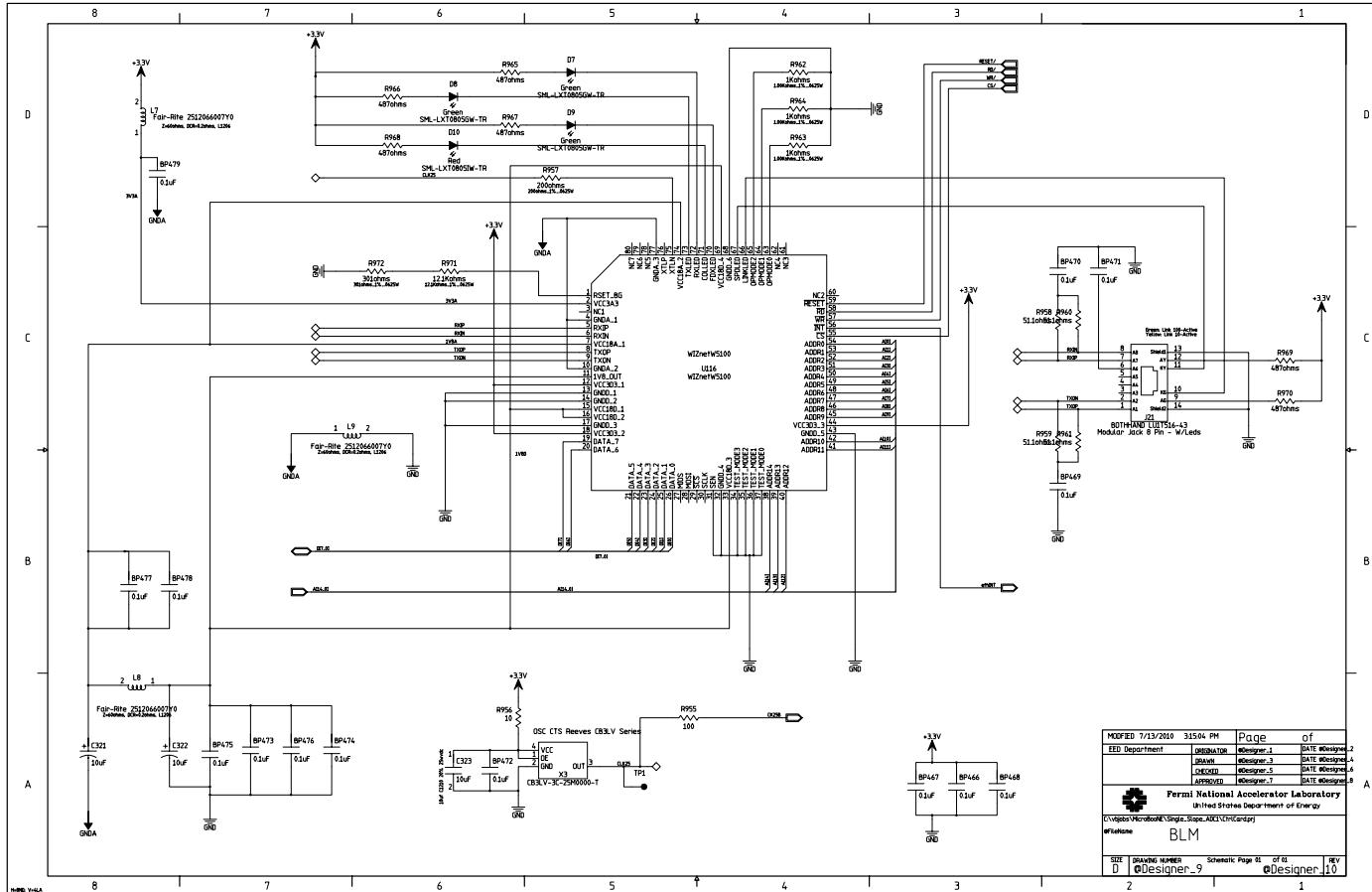
Ethernet Control



The old Ethernet controller had two separate stages:

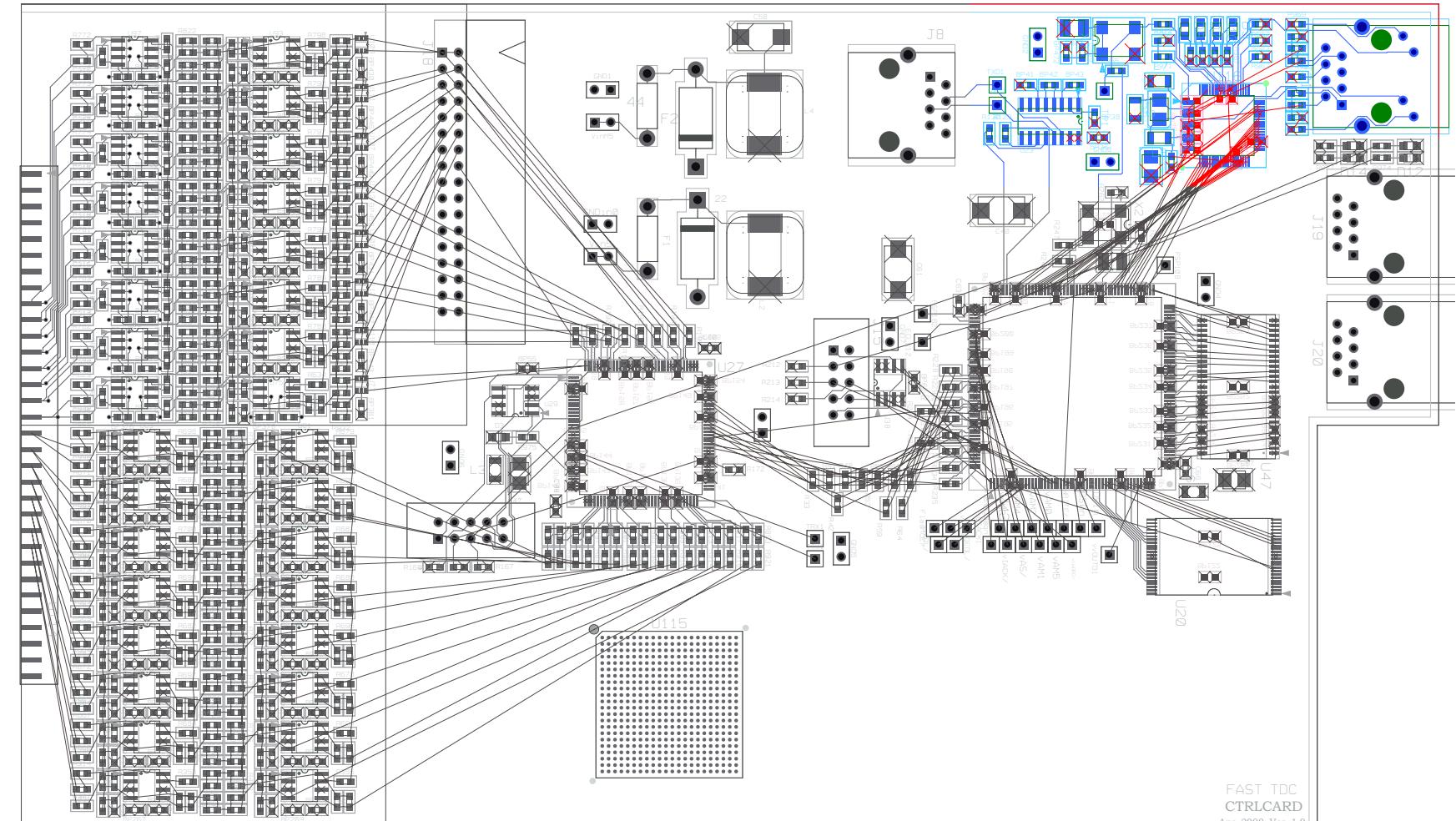
Internet connectivity chip & Physciever chip.

Ethernet Control



The new Ethernet controller uses the WIZnet Ethernet W5100 that allows us to replace both chips by combining their functionality and preserving their performance.

Ethernet Control



The new design and layout for the Ethernet controller saves valuable space on the control card.



Thank You for Listening!